REMARKS

Claims 1-28 are pending in this application. Claim 28 is canceled without prejudice pending the possible filing of a divisional patent application. Applicant respectfully requests reconsideration of the claims in view of the following remarks.

Applicant acknowledges the remarks by the Examiner regarding the Election of Species I, Claims 1-27. Applicant notes that the Examiner did not remark regarding the earlier requirement in the Restriction with respect to dependent claims 15 and 25, nor respond to the Applicant's arguments submitted in the Election made with respect to these dependent claims. As the Examiner has treated these claims as pending in the present Examiner's Action, including applying prior art to these dependent claims, and consistent with the claim status indications on the Office Action Summary which accompanied the Examiners' Action, Applicant concludes that these claims are pending in the case.

Claims 1-4, 7, 9, 14 and 16-17 were rejected under 35 U.S.C. §102(e) as being anticipated by Lee. Claims 5-6, 8, 10-13, and 18-24 were rejected by the Examiner under 35 U.S.C. §103 over the combination of Lee in view of Chung. Claims 15, and 25-27, were rejected under 35 U.S.C. §103 over the combination of Lee with Cheong, (Claim 15), and over the combination of Lee, Chung and Cheong (Claims 25-27). Each of these rejections is hereby respectfully traversed.

With regards to the rejection of independent method claim 1, the Examiner remarked *inter alia* that the Lee application (2003/0109140) provided the recited steps including disclosing "...a method of fabricating a semiconductor device in a substrate, forming a trench having sidewalls in the substrate, forming a silicon layer (polysilicon layer 60) along the sidewalls of the trench to continuously cover at least a portion of the sidewalls..."

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Applicant respectfully submits that this understanding of the Lee application is in error. This is not surprising considering that the text itself is incorrect. A review of the descriptions of Figures 6 and 7 in the Lee Application reveal that the numeral 60 refers to a barrier or liner, and it is apparent from the text and the figures taken together that element 62, a horizontal layer not adjacent the sidewalls, is in fact intended to illustrate the silicon layer (polysilicon) of Lee.

This understanding was confirmed when the resulting corresponding U.S. Patent, U.S. Patent No. 6,759,335, issued July 6, 2004 (listed in the accompanying PTO/SB/08a), was compared to the Lee application. In the patent specification, the silicon (polysilicon layer) described by Lee has been correctly identified as element 62, the text now recites:

> A silicon nitride liner or other barrier layer may be formed using chemical vapor deposition (CVD) or atomic layer deposition (ALD) methods. This liner layer 60, not shown, is formed within the collar divot 55. The liner layer may have a thickness of between about 5 and 30 nm. The liner layer is optional to the process of the invention. The liner layer suppresses excess out-diffusion of dopants into the source/drain region and to prevent dislocation in the silicon layer, which may cause leakage. The liner layer is optional in the HSG process because HSG will not grow on crystalline silicon due to lack of surface mobility of silicon atoms.
>
> Now, a buried strap is formed by a selective deposition process. A conductive layer is deposited selectively. This layer must serve as a dopant source. A selective hemispherical grain (HSG) method is preferred. If a HSG method is not used, another selective deposition method such as SiGe, selective polysilicon, or pseudo-epitaxial silicon methods may be used.
>
> The preferred selective HSG polysilicon process will now be described. Preferably, the optional surface amorphization step by plasma doping has been performed to provide surface mobility of the silicon atoms in 54 to promote HSG formation. Now, selective HSG 62 is formed as is conventional in the art for stacked capacitor applications, as shown in FIG. 6.
>
> The polysilicon 62 (or other conductive layer) can be doped in-situ during or immediately after the deposition step.

(Col. 3 lines 50-67, and Col. 4, lines 1-11).

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Thus, Lee provides a horizontal layer of silicon 62, but does not disclose a silicon layer formed on sidewalls as recited in the method steps of Claim 1.

As the reference does not show, teach or suggest the steps of Claim 1, Applicants believe Claim 1 is allowable over the rejection. Accordingly reconsideration and allowance are requested.

Claims 2-4, 7, 9, 14 and 16-17 depend from and add limitations to the method of Claim 1 and incorporate the allowable steps of Claim 1. Accordingly these dependent claims are also believed to be allowable, and reconsideration and allowance are therefore requested.

Claims 5-6, 8, and 10-13 were rejected under §103 over the combination of Lee, discussed above, and Chung (U.S. Patent No. 6,734,106). Each of these claims depends from Claim 1 and recites additional steps, which the Examiner admits are not shown in Lee. The Examiner then proposes to combine Lee with the process parameters of Chung, and for some steps, made additional arguments that certain steps do not require undue experimentation, or, are design choices, are obvious over the combination of the two references.

Applicant respectfully responds. Without agreeing with or acceding to the Examiners assertions about whether certain specific method steps could be said to be obvious even though these steps are not shown by the combined prior art references, Applicant submits that the combination relied upon by the Examiner fails to obviate the claimed methods under 35 U.S.C. §103. Each of these dependent methods incorporates the allowable steps of Claim 1, which are not shown in Lee, and the second reference, Chung, also fails to disclose the steps of Claim 1 or otherwise correct the deficiencies in Lee; thus, these dependent claims are also allowable. Reconsideration and allowance are therefore requested.

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With regards to Claims 18-24, Claim 18 is another independent method claim, which recites novel steps for forming a silicon layer to continuously cover a node dielectric, where the node dielectric lines the sidewalls in a trench having sidewalls formed in a substrate. Applicant submits that similarly to the arguments made with respect to Claim 1 above, Applicant believes that Lee does not teach the required method steps, and that therefore Lee does not show, teach or suggest the method of Claim 18. The gas phase dopant process parameters provided by Chung do not correct or provide the missing steps in Lee, and Applicant believes independent Claim 18 is allowable over the rejection. Claims 19-24 depend from and incorporate the steps of Claim 18 and these dependent claims are therefore also believed to be allowable over the proposed combination of references. Reconsideration is requested.

Claims 15 and 25 -27 recite ex-situ processing as method steps, in addition to the methods of Claim 1 (with respect to dependent claim 15) and 18 (with respect to claims 25-27). The Examiner asserted that these claims are obvious under 35 U.S.C. §103 over a combination of Lee and the ex-situ processing of Cheong (Claim 15) or over the combination of Lee, Chung and Cheong (Claims 25-27). Applicant again submits that both of the independent claims are allowable, and that the proposed combination of references does not provide the elements of these claims. Thus, these dependent claims, which incorporate the allowable method steps of the parent claims, are also allowable over the proposed combinations relied upon by the Examiner. Accordingly, reconsideration and allowance are requested.

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Applicant has made a diligent effort to place the claims in condition for allowance. However, should there remain unresolved issues that require adverse action, it is respectfully requested that the Examiner telephone Mark E. Courtney, Applicant's attorney, at 972-732-1001 so that such issues may be resolved as expeditiously as possible. No fee is believed due in connection with this filing. However, should one be deemed due, the Commissioner is hereby authorized to charge Deposit Account No. 50-1065.

Respectfully submitted,

4/10/2006
Date

Mark E. Courtney
Attorney for Applicant
Reg. No. 36,491

Slater & Matsil, L.L.P.
17950 Preston Rd., Suite 1000
Dallas, Texas 75252-5793
Tel. 972-732-1001
Fax: 972-732-9218

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